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NON-LINEAR EFFECTS IN VARACTOR TUNED RESONATORS

Liang Zhou and Jeremy Everard

Department of Electronics, University of York, York, YO10 5DD, UK

Abstract –**This paper describes the effects of RF power level on the performance of varactor-tuned resonator circuits. A variety of topologies are considered including series and parallel resonators operating in both unbalanced and balanced modes. As these resonators were being designed to produce oscillators with minimum phase noise the insertion loss was set to 6dB and hence Q_L/Q_0=1/2. To enable accurate analysis and simulation, accurate S parameter and PSPICE models for the varactors were optimised and developed. It is shown that these resonators start to demonstrate non-linear operation at very low power levels demonstrating saturation and lowering of the resonant frequency. On occasion 'squegging' is observed for modified biasing conditions. The non-linear effects are dependent on the Q, bias voltage and circuit configurations with typical non linear effects occurring at –6dBm in a circuit with a loaded Q of 63 and a varactor bias voltage 3 volts. Analysis, simulation and measurements are presented which show close correlation.**
Keywords- **VCOs, Varactors,**

I. INTRODUCTION

The requirements for accurate tuning of VCOs with low phase noise is very important in oscillator design. As the phase noise is inversely proportional to Q^2 and the power in the resonator, high power and high Q would often be preferable.

Due to the Q of the resonator the RF voltage applied to the resonator becomes multiplied across the varactor often causing unwanted effects in the oscillator and thereby setting the phase noise in the oscillator.

Many workers have investigated these effects, see for example [4] [5], however the effects are often not quantified very accurately due to a wide variety of design rules and the fact that the resonator is usually already incorporated into the oscillator.

In this paper the tunable resonators were designed to operate as if they were in an oscillator optimised for minimum phase noise. This requires Q_L/Q_0 = ½ thus setting S_{21} = -6dB. However they are built separately and can therefore be investigated independently. Simulations and measurements are performed on VHF circuits using a BB833 varactor diode.

This paper is ordered as follows. Section ii describes the low phase noise theory. Section iii describes the linear theory for power handling in varactor based resonators. Section iv describes the varactor diode models and section v describes the resonator designs. Section vi describes measurements and simulations and section vii describes 'squegging' under certain operating conditions.

II. PHASE NOISE THEORY

It is important to develop a simple model to calculate and predict the noise performance of an oscillator. A suitable model is shown in figure 1. This consists of an amplifier with two inputs which are added together. These represent the same input but are separated to enable one to be used for the noise input and the other for feedback. The resonator is represented as an LCR circuit where any impedance transformation is achieved by varying the component values. This circuit operates as a Q multiplication filter but also contains the additional constraint that the AM noise is removed. The model is put in this form to highlight all the effects, which often do not show up in a block diagram model.

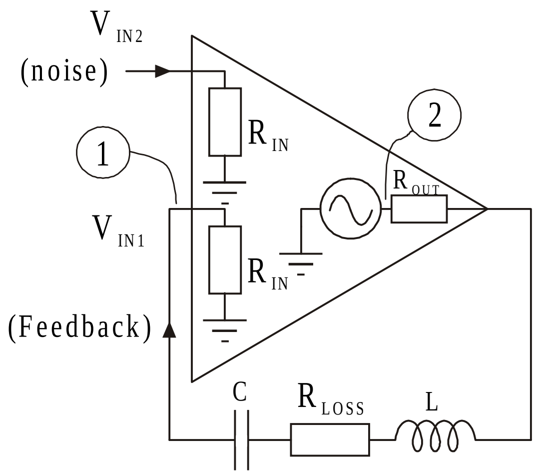

Figure 1 Oscillator model

A general equation for the phase noise can be derived as shown in equation 1 [1] which allows for a number operating conditions including power and the output and input impedances.

Equation 1:

$$L_{FM} = A \cdot \frac{FkT}{8\left(Q_0\right)^2 \left(Q_L/Q_0\right)^2 \left(1 - Q_L/Q_0\right)^N P} \left(\frac{f_0}{\Delta f}\right)^2$$

where:

1. $N = 1$ and $A = 1$ if P is defined as P_{RF} and R_{OUT} = zero.
2. $N = 1$ and $A = 2$ if P is defined as P_{RF} and $R_{OUT} = R_{IN}$.
3. $N = 2$ and $A = 1$ if P is defined as P_{AVO} and $R_{OUT} = R_{IN}$.

And P_{RF} is the total power dissipated in the output, input and loss resistances and P_{AVO} is the power available at the output of the amplifier.

If we take expansion 3 and show the full equation including the impedances, we obtain equation 2 [1].

Equation 2:

$$L_{FM} = \frac{FkT}{32 Q_0^{\,2} \left(Q_L / Q_0\right)^2 \left(1 - Q_L / Q_0\right)^2 P_{AVO}} \left(\frac{\left(R_{OUT} + R_{IN}\right)}{R_{OUT} \, . R_{IN}}\right) \left(\frac{f_0}{\Delta f}\right)^2$$

$$\text{Under optimum conditions} \rightarrow \frac{2FkT}{Q_0^{\,2} P_{AVO}} \left(\frac{f_0}{\Delta f}\right)^2$$

This is minimum when $R_{OUT} = R_{IN}$ and $Q_L/Q_0 = ½$ and hence when the insertion loss of the resonator is –6dB. This minimum occurs because the amplifier gain is set by the insertion loss of the resonator which is $S_{21} = (1-Q_L/Q_0)$. This optimum value for Q_L/Q_0 is also described by Parker in a paper on SAW oscillators [3]

III POWER HANDLING OF GENERAL RESONATOR

The noise performance of a broad tuning range oscillator is usually limited by the Q and the voltage handling capability of the varactor as has been described by Underhill [5]. These equations were extended to include oscillators operating under optimum conditions [1] and are extended here for general conditions which relate this voltage to the coupling coefficient and hence Q_L/Q_0. This is examined by taking a simple model for the resonator as shown in Figure 2.

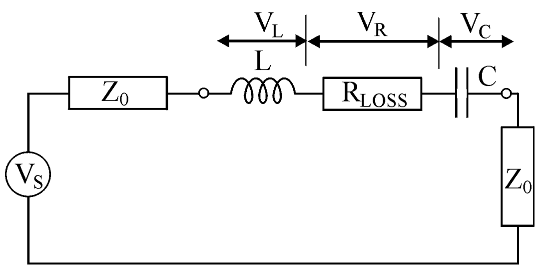

Figure 2 General model for resonator

The power dissipated in the varactor is:

$$P = \frac{V_{R_{LOSS}}^{\;\;2}}{R_{LOSS}}$$

The voltage across the capacitor V_C in a resonator is:

$$V_C = Q V_{R_{LOSS}}$$

Therefore the power dissipated in the varactor is:

$$P_V = \frac{V_c^{\,2}}{Q^2 R_{LOSS}}$$

The voltage across the varactor can also be calculated in terms of P_{AVO} and Q_L/Q_0 by using:

$$P_{avo} = \frac{V_s^{\,2}}{4 Z_0} \qquad\qquad P_{Varactor} = \frac{(V_{R_{LOSS}})^2}{R_{loss}}$$

So

$$V_s^{\,2} = 4 Z_0 P_{AV0}$$

From Figure 2:

$$Q_L = \frac{\omega L}{R + 2Z_0} \qquad Q_0 = \frac{\omega L}{R} \qquad \therefore \frac{Q_L}{Q_0} = \frac{R}{R + 2Z_0}$$

$$V_R = V_S \cdot \frac{R}{R + 2Z_0} = \left(\frac{Q_L}{Q_0}\right) . V_s$$

$$\text{As: } P_{Varactor} = \frac{(V_{R_{LOSS}})^2}{R}$$

$$\therefore P_{Varactor} = 2 \frac{Q_L}{Q_0} . \left(1 - \frac{Q_L}{Q_0}\right) . P_{AVO}$$

When $Q_L/Q_0 = 1/2$, $P_{AVO} = 2P_V$ [8], the noise performance is then set totally by the varactor loss resistance and the voltage handling capability to be:

$$L_{FM} = \frac{FkTR_{LOSS}}{V_C^{\,2}} \left(\frac{f_0}{\Delta f}\right)^2$$

It will be shown later that the resonator starts to distort at a power level of –6dBm, so $P_{avo} = 0.251\times10^{-3}W$

$$\therefore P_{avo} = 2P_V = 2\times\frac{V_R^{\ 2}}{R_{loss}} = 2\times\frac{V_R^{\ 2}}{2} = V_R^{\ 2}$$

V_R is voltage across the resistance of the varactor.

$$\therefore V_R = 1.58\times10^{-2}V$$

$$V_{Rrms} = \sqrt{2}\times V_R = 2.24\times10^{-2}V$$

As the loaded Q is:

$$Q_L = 63 \quad \text{then} \quad Q_0 = 126 \quad (Q_L / Q_0 = 1/2)$$

The voltage across the varactor would be:

$$V_C = Q_0 \times V_R \approx 3V$$

This RF voltage is now the same as the DC bias voltage for the varactor in our experiments so one would start to expect non linear effects.

IV VARACTOR DIODE MODELS

A. Small signal model

To obtain an accurate model for the varactor a small signal AC model is developed initially. This information can then be used to optimise the large signal model. This AC model consists of a series LCR circuit as shown in Figure 3.

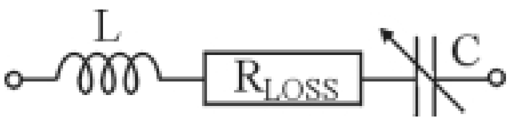

Figure 3. Simple LCR varactor model

The model was optimised using the S parameters for a DC bias of 3V. The S parameters and the modelled S parameters were optimised for close agreement up to 1GHz as illustrated in Table 1 and Figures 4 and 5. At 3 volts the values for this model are, L = 1.8nH, C= 4.8pf and R_{LOSS} = 2Ω.

Table I

S Parameters comparison between model and actual results

Frequency	S(1,1)				Optimized resistance
	Optimizations		Actual results		
	MAG	ANG	MAG	ANG	
50Mhz	0.99952	-8.72	0.99935	-8.8	2.081
100Mhz	0.99810	-17.3	0.99794	-17.5	2.081
150Mhz	0.99582	-25.9	0.99603	-26.0	2.081
200Mhz	0.99277	-34.3	0.99253	-34.5	2.081
250Mhz	0.98911	-42.5	0.98940	-42.7	2.081
300Mhz	0.98497	-50.4	0.98497	-50.6	2.081

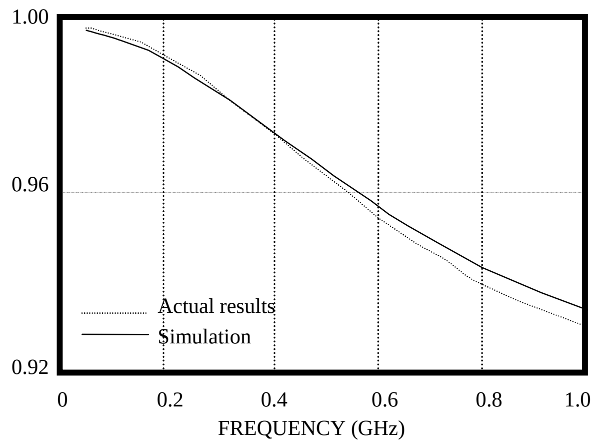

Figure 4 Magnitude of S_{11} in simulation and measurements

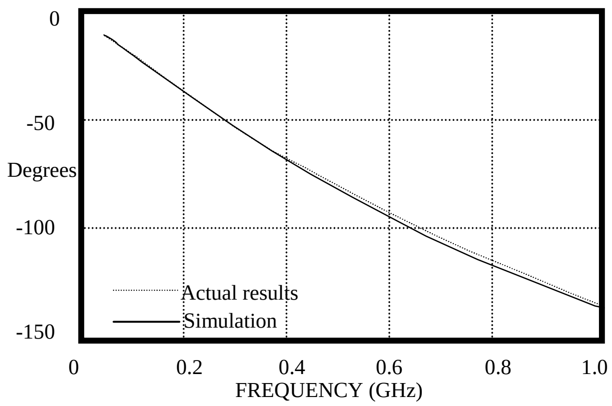

Figure 5 Phase of S_{11} in simulation and measurements

B. PSPICE Model

Initially we started to develop our own PSPICE model [6]. For a step (abrupt) junction, or linearly graded junction, the capacitance could be approximately defined as:

$$C = \frac{C_{jo}}{(1-\frac{V_j}{\phi})^M}$$

Where C_{j0} is the zero-bias value, ϕ is the junction barrier potential, and M is the grading coefficient, varying M will generate a variety of reverse bias capacitance characteristics, V_j is the zero bias depletion region capacitance.

However a SPICE model was then obtained from Infineon which appeared very accurate except for the fact that the series resistance appeared too low resulting in rather large Q values. Based on the AC measurements this resistance was changed to 2Ω and the results were then much more accurate.

The parameters for BB833 were: IS = 113.2f, N = 1.22, Rs = 120.0m, XTI = 3.0, EG = 1.16, C_{jo} = 14.79, M=1.464, Vj=2.594, FC=0.5, TT = 120.0n, BV = 32, IBV=1.0n.

C. Simulation Comparison with Actual Results

Figure 6 shows the capacitance Vs reverse voltage for both simulation and measurements. The real part (resistance value) and imaginary part (capacitance value) are examined by modelling the circuits including BB833 package model using the circuit shown in Figure 7. The varactor diode BB833 is operated at DC bias voltage 3 volts, large capacitors and inductors are used to block DC and AC voltages. The resistance value is nearly 2ohm (real part shown in Figure 8, The capacitance value could be derived by 1/jωC at 100Mhz (imaginary part shown in Figure 9 where the value is 4.9PF which is close to 4.86PF (actual value) at DC bias voltage of 3volts.

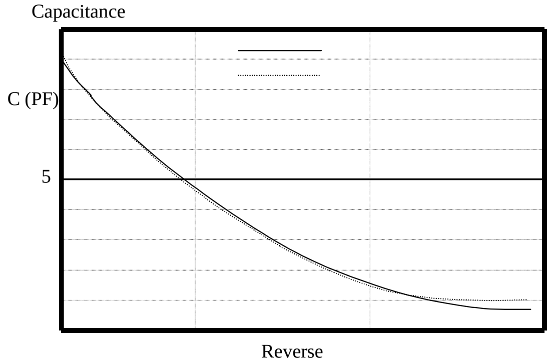

Figure 6. Capacitance Vs Reverse Voltage

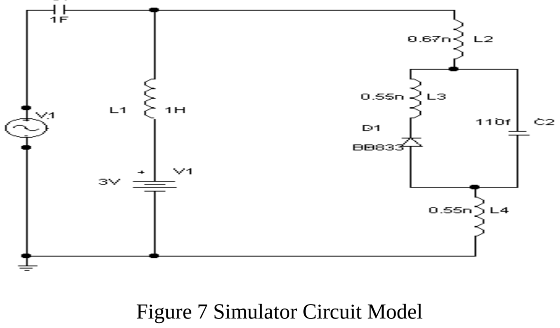

Figure 7 Simulator Circuit Model

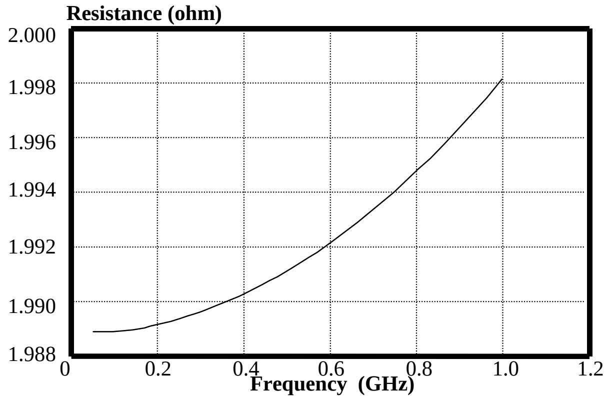

Figure 8. Real part of impedance for BB833

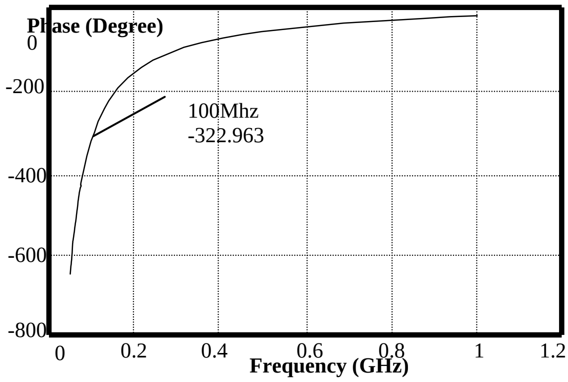

Figure 9 Imaginary part of impedance for BB833

V. RESONATOR DESIGNS

To investigate the non-linear effects, a variety of resonator topologies have been simulated and measured at the same DC bias voltage. This includes unbalanced series and parallel resonators and a balanced parallel resonators with two varactors. All these designs are based on the insertion loss of –6dB at the center frequency under the DC bias voltage of 3volts. The insertion loss of course varies with the tuning voltage.

A. Unbalanced Series Resonators

A 140Mhz unbalanced series resonator is shown in Figure 10. This circuit contains an inductor with series resistance 1ohm and a varactor diode BB833. Two DC blocking capacitors C_3 and C_5 are used. Capacitors C_1 and C_2 are used to obtain the correct ratio of Q_L/Q_0 and the resistors are used to apply DC bias at low impedance points.

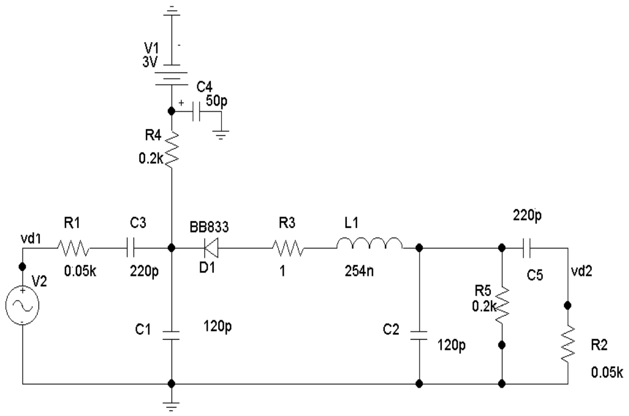

Fig.10. 100Mhz unbalanced series resonator schematics

The design of the resonator is achieved using the following rules, as are largely described in [1] however the varactor loss resisistance is also included here.

1. Model the resonator as a series LCR circuit as shown in Figure 11.

2. Merge all the loss resistances of the varactor and the inductor and capacitor into R_{LOSS}.

3. Set S_{21} = -6dB (Q_L/Q_0 = ½) by making the source resistance seen by the resonator, $Z_0 = R_{LOSS}/2$ as shown in Figure 12.

4. Design LC matching network to achieve 3 (Figure 13).

5. As the inductor you will use is L, subtract 2L’ from L and calculate the value of C for the resonant frequency.

6. Now incorporate 2L’ into L to make the total value = L.

7. The final circuit is shown in Figure 14. It should be noted that the value of C_S is often rather large and that parisitic inductances often increase the equivalent value. Add a parisitic inductance and then reduce C to achieve correct QL/Q0.

8. Incorporate DC bias by adding ‘lowish’ value resistors at the low impedance points which are at the input and output as shown in Figure 10. These resistors should be fairly low to ensure that they do not degrade the noise performance of the oscillator [1].

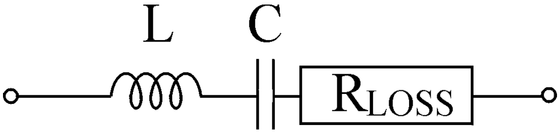

Figure 11 LCR Model

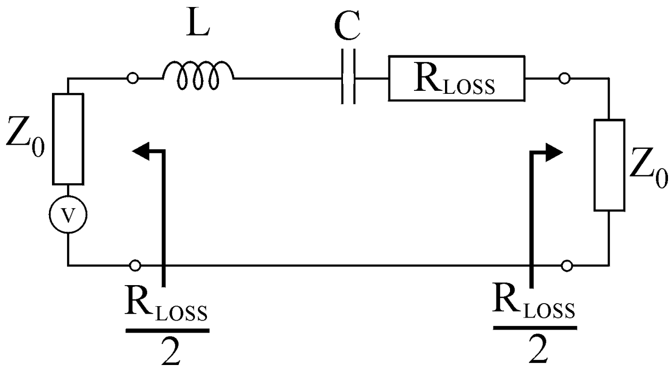

Figure 12 Make source resistance = $R_{LOSS/2}$

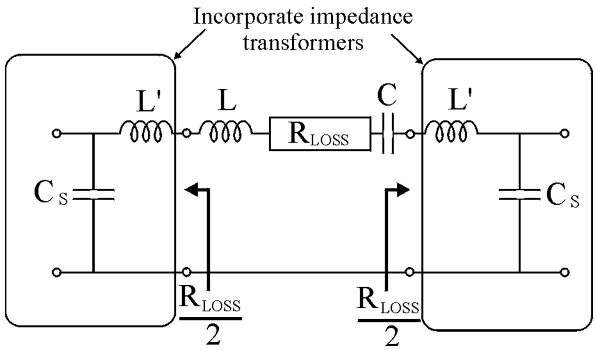

Figure 13. Resonators with impedance transformers

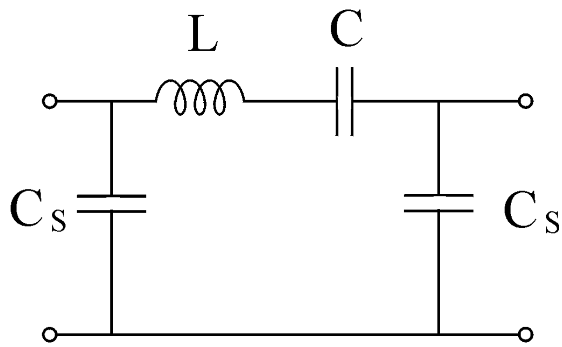

Figure 14. Final Resonator

D. Unbalanced Parallel Resonators

The parallel resonators are designed using the same method as the series resonators, however now the resonator is a parallel resonator and the impedance transformers are tapped C as shown in Figure 15. The loaded Q of this circuit is 63.

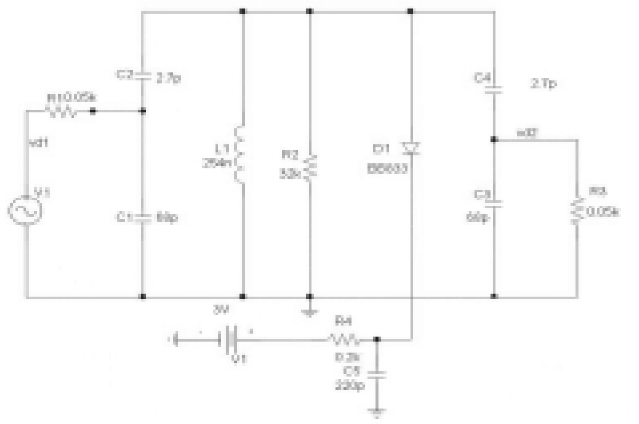

Figure 15. Unbalanced Parallel Resonator

E. Balanced Parallel Resonators

Balanced parallel varactors resonators are based on two unbalanced resonators (Figure 16). The advantage of this circuit is that it contains a double back to back diode and being balanced the even harmonic distortion is suppressed. Two center-tapped transformers have been used to enable these circuits to be measured using an unbalanced network analyzer. The insertion loss is again set to –6dB at DC bias voltage 3volts, where the loaded Q is about 40. The frequency tuning range is from 92.6Mhz to 122.2Mhz.

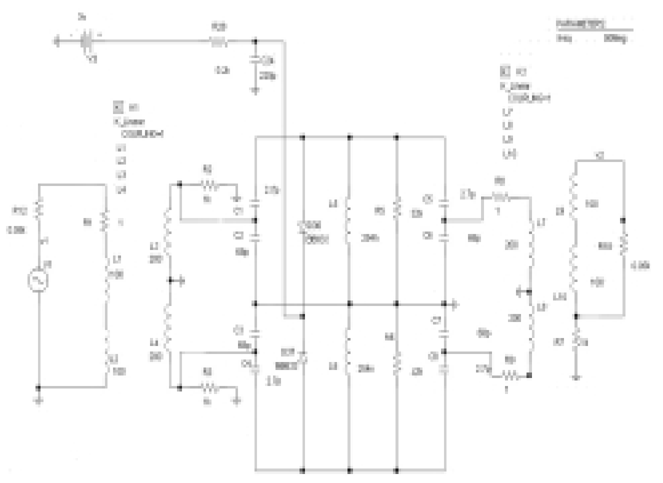

Figure 16. Balanced Resonator

VI MEASUREMENTS AND SIMULATION

A measurement system is shown in Figure 17. A network analyser is combined with a variable attenuator and medium power amplifier (MINICIRCUIT ZFL-1000VH with a +25dBm 1dB gain point). The two 10dB attenuators are used to protect the network analyzer.

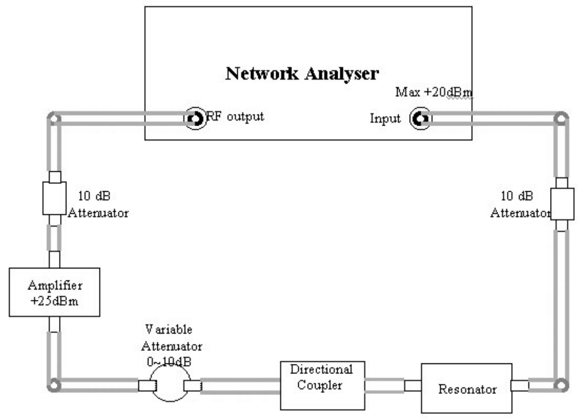

Figure 17. Measurement System

The frequency response at different power levels is shown in Figure 18. Similar results were obtained for the unbalanced series and parallel resonators. Distortion starts to occur at around –5dBm.

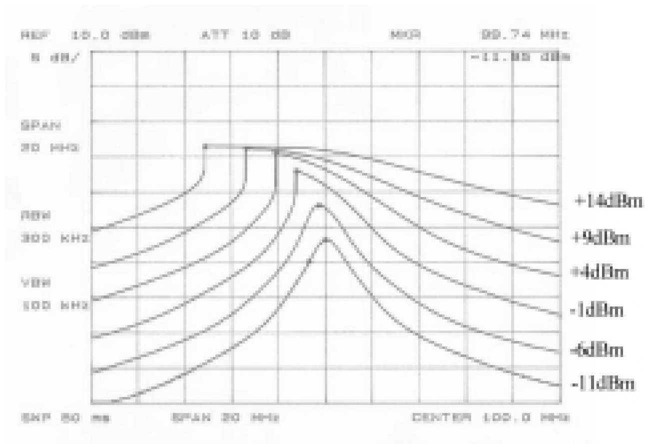

Figure 18 Distortion with increasing power into resonator.

The response for the balanced parallel resonator is shown in Figure 19 the power at which distortion starts to occurs is around +3dBm. This is because the circuit now contains a double back to back diode and, being balanced, the even harmonic distortion is suppressed.

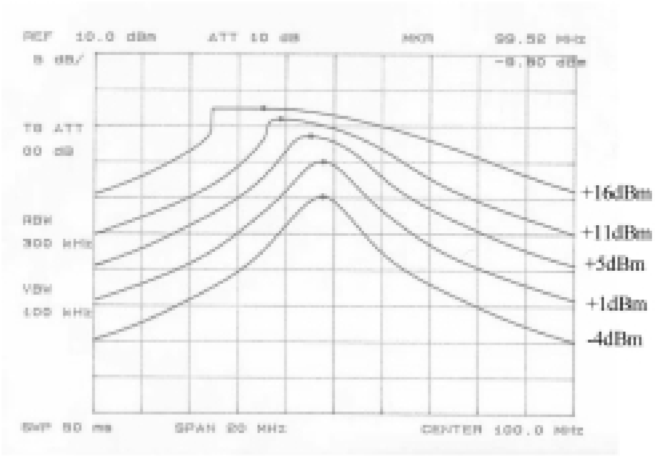

Figure 19 Distortion in balanced parallel resonator

This distortion is caused by the fact that as the RF power increases this increases the average capacitance. This is because the increase in capacitance at lower voltages is larger than decrease at higher voltages. The increase in average capacitance therefore lowers the resonant frequency. The sharp transition is due to the sudden rise in voltage across the varactor as resonance is approached.

PSPICE was used to simulate the circuits in both the frequency and the time domain. Initially this was performed at low RF power levels and as expected the AC response is identical to the time domain response as shown in Figure 20.

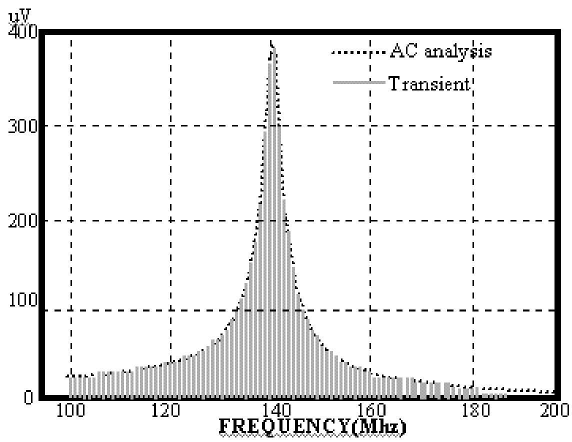

Figure 20 Linear and non-linear modelling at low power

The RF power level was then increased and the distortion effects are then seen as shown in Figure 21. The time domain response was taken by incrementally increasing the input frequency in 5 MHz steps after waiting for the waveform to settle at each point. The FFT option was left-on providing the plots. In fact a slow sweep could also have been implemented.

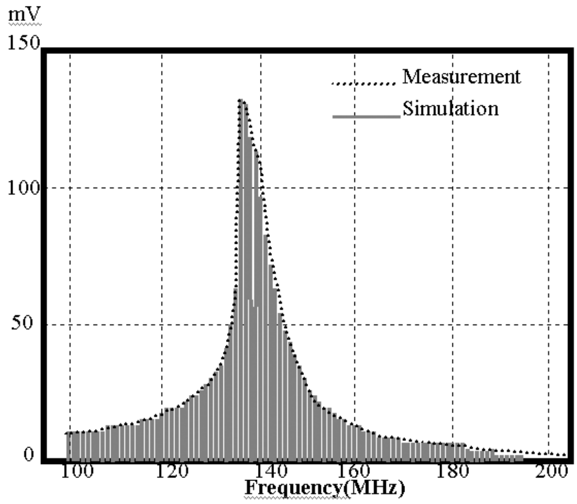

Figure 21. Transient analysis and measurements at a P_{AVO} power level of –5dBm.

VII. SQUEGGING

There is an interesting power response for the balanced parallel resonators if the DC biasing resistor is increased to 10kΩ and the de-coupling capacitor is removed. The frequency response is shown in Figure 22 and the time domain response is shown in Figure 23. The squegging response shown is when the P_{AVO} power level is +5dBm with a DC bias voltage 2.78volts. This 'squegging' occurs when the source frequency is within the flat top of the frequency response.

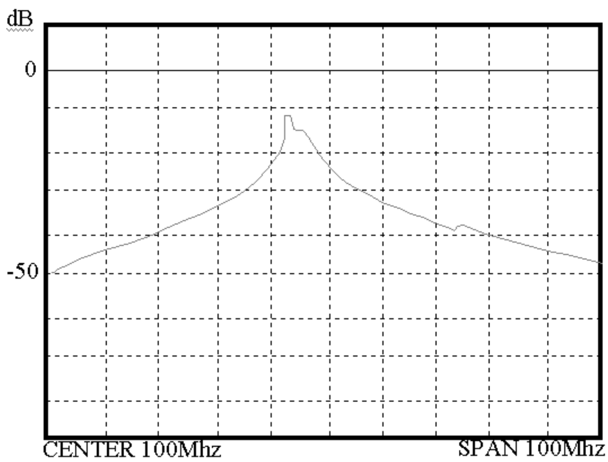

Figure 22 Frequency response of 'squegging' circuit

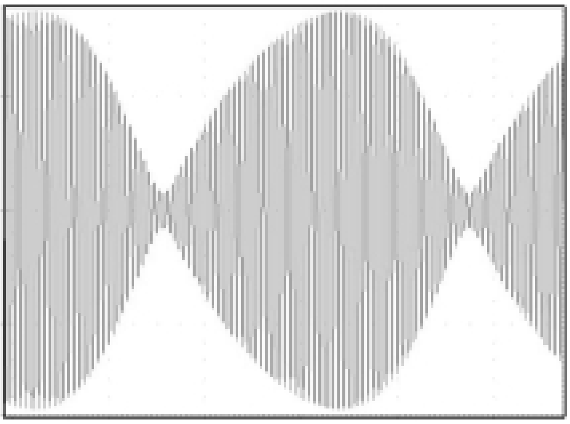

Figure.23. Squegging across the varactor in unbalanced resonators

VIII. CONCLUSIONS

Several different varactor based resonators have been analyzed, simulated and measured and initial results presented. It is shown that a simple AC analysis agrees with the transient analysis and that large signal measurements and simulation show close correlation.

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